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09/821,421	03/29/2001	Michael W. Williams	PW 027 5033 P11012	3663

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EXAMINER	
WU, IVES J	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,421	WILLIAMS ET AL.	
	Examiner	Art Unit	
	Ives Wu	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *5/20/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-11,14-20,23* is/are rejected.

7)☒ Claim(s) *5,6,12,13,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(1). Claims 1-4,8-11,15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Barth et al (US006154821A).

As to claim 1, Barth et al (US006154821A) teach by citing "Operation continues at step 1405, at which the channel or bus population is checked or determined. At this step, the number of DRAM devices coupled to the bus is determined" (Column 13, line 11-13) **[Claim 1: A method of handling memory read return data from different time domains, comprising: determining a number of distinct memory device ranks]**, "In one embodiment, the levelizing comprises determining the response time **[time domain]** of each of the DRAM devices coupled to the bus using information communicated over at least one bus"(Column 17, line 46-49) **[claim 1: determining a time domain for each of the distinct memory device ranks]**, "Operation continues at step 1428, at which the read domains of the DRAM devices are levelized" (Column 17, line 7-8), "Operation continues at step 1429, **[corresponds to claim 1: scheduling a transaction based on the time**

domain for each of the distinct memory device ranks] at which the minimum offset is determined between a read SCP and a subsequent write SCP"(Column 10, line 10-12) **[corresponds to claim 1: so that at least one of data collisions and out-of-order data returns are prevented]** because applicant cites "Moreover, because levelization prevents out-of-order data returns from occurring" (applicant's Specification, page 3,line 9-10).

Claim 8 (system) is rejected for the same reason applied to claim 1.

Claim 17 (machine-readable medium) is rejected for the same reason applied to claim 1.

(2). As to claim 2, Barth et al (US006154821A) teach by citing "3. Determine the round trip delay time from the controller's point of view of a READ to the first device....Parameter cycREADrdram is the sum of theses two times. Parameter cycPROPrdram is the first value and parameter 7+cycCLSsys + cycDACspd is the second value. 4. Compute the first value from the round trip delay and normalize device values of tCLS and tDAC"(Column 18, line 12-22). Because roundtrip time reflects the distance between memory unit and memory controller, the relative position is determined based on shortest roundtrip time of first memory device and longest roundtrip time of another memory device (Column 18, line 29-30). **[claim 2: The method according to claim 1, further including determining a relative position of each of the distinct memory device ranks]**.

Claim 9 (system) is rejected for the same reason applied to claim 2.

Claim 18 (machine-readable medium) is rejected for the same reason applied to claim 2.

(3). As to claim 3, Barth et al (US006154821A) teach by citing "In one embodiment, in order to determine the number of DRAM devices coupled to the channel, configuration information stored in the SPDs indicates the number of DRAM devices on each module, and the sum total determines how many are coupled to the channel" (Column 13, line 17-22) **[Claim 3: The method according to claim 1, wherein the determining of the number of the distinct memory device ranks is performed utilizing Serial Presence Detect (SPD)]**.

Claim 10 (system) is rejected for the same reason applied to claim 3.

Claim 19 (machine-readable medium) is rejected for the same reason applied to claim 3.

(4). As to claim 4, Barth et al (US006154821A) teach by citing "2. Write all ones data to the first device on the channel"(Column 18, line 11) **[claim 4: The method according to claim 1, wherein the determining of the time domain for each of the distinct memory device ranks includes: writing a predetermined data pattern to a memory device rank to be tested]**, "The memory controller then measures the elapsed time between the issuance of the read

command and receipt of the logic one from the memory location of the DRAM device"(Column 17, line 56-60)**[claim 4: reading back the predetermined data pattern]**, "3. Determine the roundtrip delay time from the controller's point of view of a read to the first device"(Column 18, line 12-13) **[claim 4: receiving the predetermined data pattern, assuming that the time domain of the memory device rank to be tested is in a first time domain;]**. Because Barth et al (US006154821A) disclose measurement of roudtrip time when the logic ones are received, Logically, the "receipt of data" implies that the data pattern must be checked to be correct in order to clock the receipt time, if the data received is not correct pattern is the same meaning of not receiving the response from the tested memory device. Naturally, timing will continue until memory controller receives the correct pattern data so that the elapsed time for the memory device will be determined. **[claim 4: determining whether the predetermined data pattern was correctly received; increasing the time domain of the memory device rank to be tested by at least a clock if the predetermined data pattern was not correctly received; and establishing the time domain for the memory device rank to be tested once the predetermined data pattern is correctly received]**.

Claim 11 (system) is rejected for the same reason applied to claim 4.

Claim 20 (machine-readable medium) is rejected for the same reason applied to claim 4.

(5). As to claim 15, Barth et al (US006154821A) teach by presenting figure 2,120 (bus) and cite "One set of connections forms a bus 120 or channel over which information is passed between the memory controller 120 and all DRAM devices 110-116"(Column 4, line 60-63)**[claim 15: The memory system according to claim 8, where the connection is a bus]**.

(6). As to claim 16,Barth et al (US006154821A) teach "while the operations comprising writing data to and reading data from the DRAM devices are performed over the bus 120" (Column 6, line22-25) "The first offset circuit 150 is configured to determine a minimum clock cycle offset between a READ command and a subsequent WRITE command communicated to the DRAM devices 110-116 over the main channel 120" (Column 5, line34-37) **[claim 16: The memory system according to claim 15,wherein the bus includes a data bus and an address/command bus]**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

(7). Claim 7,14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barth et al (US006154821A), in view of Stracovsky et al (US006587894B1).

Although Barth et al (US006154821A) teaches to measure the elapsed time by issuing a READ command after a WRITE command to the memory units and a levelization method is disclosed, but he fails to teach to solve data contention conflicts without using levelization.

However, Stracovsky et al (US006587894B1) teach by citing "In this way, the universal controller 904 is capable of dynamically scheduling the issuance of SLDRAM command packets based at least upon particular destination address device operating characteristics as well as the current state of the command and data packet stream."(Column 14, line 41-45) **[corresponds to claim 7: The method according to claim 1, wherein the scheduling of the transaction includes:]**, "Once the physical constraints of the resource are determined for a

particular universal command component, a determination is made at 606 whether or not there are additional command components included in the universal command" (Column 10, line 49-53) **[claim 7: determining whether a new request is available]**, "In the described embodiment, the collision detector 2002 detects all possible data collisions between a "to be issued" command (that is stored in a command queue 2004) and "already issued" commands (that are stored in a data queue 2006)" (Column 26, line 8-12). **[Claim 7: determining whether there are pending or outstanding transactions if the new request is available; consulting a history of pending or outstanding transactions]**, "Before the issue of the command to the target device the new data packet ND (New Data) is checked according to it's timing information to see if it can be inserted into the data queue without collision" (Column 26, line 40-44) **[Claim 7: determining whether a data contention conflict exists]**, "Fig. 20 illustrates a collision detection system 2000 that is another implementation of the collision detection system 1500 shown in FIG. 15. In this embodiment, the collision detection system 2000 reorders commands to achieve an optimal command sequence based on target response restrictions and determines the optimal slot for data transfer between initiator controller and target subsystem. Because the reordering of the commands can not cause collision of different data packets on the data bus, a collision detector 2002 that prohibits o the issuance of a particular command if the command data transfer related to this particular command would cause data conflict is required" (Column 25, line 60 – column 26, line

7) **[claim 7: determining whether the data contention conflict may be resolved by scheduling the transaction now and sending the transaction later if the data contention conflict exists]**, "This particular example illustrates collision detection of the memory controller that supports both non-burst and burst data transfer (i.e., 4 data stream). Due to the bi-directional nature of the data bus, one clock cycle must be inserted between consecutive read-write or write-read transfers" (Column 26, line 54-58), **[claim 7: waiting at least a clock if the data contention conflict cannot be resolved by scheduling the transaction now and sending the transaction later;]**, "The queues and controller unit 2010 also calculates the new issue time of commands and a time when the data appears on the data bus" (Column 26, line 30-32)," **[claim 7: scheduling the transaction if the data contention conflict may be resolved by scheduling the transaction now and sending the transaction later]**, "A command may be issued to the command bus from any one of command queue elements 1602 via multiplexer 1608 if its Cd count is zero and there are no collisions on the data bus indicated"(Column 20, line 20-23) **[claim 7: scheduling the transaction if the data contention conflict does not exist]**.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was well-known in the computer art to avoid the data

contention conflict in the data bus of memory controller by rescheduling the transactions after the detection of collision is made.

With the combination of both teachings, it would provide the applicant's invention to install a scheduling of transactions for the prevention of data collision in the memory data management.

Therefore claim 7 is rejected.

Claim 14 (system) is rejected for the same reason applied to claim 7.

Claim 23 (machine-readable medium) is rejected for the same reason applied to claim 7.

Allowable Subject Matter

(8). Claims 5,6,12,13,21,22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ives Wu whose telephone number is 571-272-4182. Examiner can normally be reached 8:00 – 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Ives Wu
Art Unit: 2186

PIERRE BATAILLE
PRIMARY EXAMINER